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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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*Ex parte* GHOLAMREZA CHAJI[1]

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Appeal 2016-002319
Application 13/470,059
Technology Center 2600

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Before MICHAEL J. STRAUSS, DANIEL N. FISHMAN, and JAMES W. DEJMEK, *Administrative Patent Judges*.

FISHMAN, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant appeals under 35 U.S.C. § 134(a) from a Final Rejection of claims 1–13 and 15–43.[2] Claim 14 has been canceled. We have jurisdiction over the pending claims under 35 U.S.C. § 6(b).

We affirm-in-part.

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[1] Appellant identifies Ignis Innovation, Inc. as the real party in interest. Appeal Brief 2.

[2] In this Decision, we refer to Appellant's Appeal Brief ("App. Br.," filed June 25, 2015); Appellant's Reply Brief ("Reply Br.," filed December 21, 2015); the Final Office Action ("Final Act.," mailed November 10, 2014); the Examiner's Answer ("Ans.," mailed on October 21, 2015); and the original Specification ("Spec.," filed May 11, 2012).

## THE INVENTION

Appellant's invention is directed to "pixel circuits including feedback capacitors and reset capacitors." Spec., Title. "The feedback capacitor generates voltage adjustments at the programming node that correspond to the variations at the emissive element, and thus reduces variations in light emission." Abstract. "A reset capacitor connected to a select line is selectively connected to the gate terminal of the driving transistor and resets the driving transistor prior to programming." *Id.*

Independent claims 1 and 22, reproduced below, are illustrative:

> 1. A pixel circuit comprising:
>
> a drive transistor including a gate terminal and arranged to convey a drive current through a light emitting device, the drive current being conveyed according to a voltage on the gate terminal;
>
> a storage capacitor connected to the gate terminal of the drive transistor;
>
> an emission control transistor connected in series between the drive transistor and the light emitting device; and
>
> a feedback capacitor connected between the light emitting device and the gate terminal of the drive transistor such that voltage changes across the light emitting device generate corresponding voltage changes at the gate terminal of the drive transistor.
>
> 22. A pixel circuit comprising:
>
> a drive transistor including a gate terminal and arranged to convey a drive current through a light emitting device, the drive current being conveyed according to a voltage on the gate terminal;
>
> a first switch transistor connected between the gate terminal of the drive transistor and a node of the pixel circuit; and
>
> a reset capacitor connected between the node and a reset line such that the reset line is capacitively coupled to the gate

terminal of the drive transistor while the first switch transistor is turned on.

## THE REJECTIONS

Claims 1–7, 12, 13, and 15–21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Uchino et al. (US 2007/0057873 A1; Mar. 15, 2007) ("Uchino") and Seto (US 2009/0244046 A1; Oct. 1, 2009). Final Act. 2–12.

Claims 22–43 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Uchino and Shibusawa (US 2010/0079419 A1; Apr. 1, 2010). Final Act. 12–26.

Claims 8–11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Uchino, Seto, and Shibusawa. Final Act. 26–32.

Claim 13 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Uchino, Seto, and Noguchi et al. (US 2005/0212787 A1; Sept. 29, 2005) ("Noguchi"). Final Act. 33–34.

Claim 36 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Uchino, Shibusawa, and Kimura (US 2001/0035863 A1; Nov. 1, 2001). Final Act. 35–36.

## ANALYSIS

Only those arguments actually made by Appellant have been considered in this Decision. Arguments that Appellant did not make in the Briefs are waived. *See* 37 C.F.R. § 41.37(c)(1)(iv).

We have reviewed the Examiner's rejections in light of Appellant's arguments that the Examiner erred. App. Br. 6–10; Reply Br. 1–7. We find Appellant's arguments in connection with the rejection of claims 40–43

persuasive of Examiner error. However, we are not persuaded by Appellant's contentions of Examiner error regarding claims 1–13 and 15–39. Accordingly, we adopt as our own the Examiner's findings and reasons set forth Final Action and the Answer solely in connection with claims 1–13 and 15–39. We highlight and address specific arguments and findings for emphasis as follows.

*Claims 1–13 and 15–21*

Regarding claim 1, the Examiner relies on Uchino for disclosing a capacitor connected to a drive transistor's gate terminal and a separate feedback capacitor connected between a light emitting device and the gate terminal. Final Act. 2–3. Specifically, the Examiner identifies capacitor C211 of Uchino's Figure 13 as disclosing the recited feedback capacitor. *Id.* at 3. The Examiner also finds capacitor C21 of Uchino's Figure 2b discloses it was known to connect a capacitor to the gate of a drive transistor as claimed. *Id.* (citing Uchino ¶ 32). The Examiner further finds, although Uchino discloses capacitor C21 coupled as recited to the gate terminal of a drive transistor, Uchino does not disclose a *storage* capacitor. *Id.* at 3. However, the Examiner finds Seto, in combination with Uchino, discloses a storage capacitor connected to the drive transistor's gate terminal. *Id.* (citing Seto ¶ 51, Fig. 2 (capacitor 11d connected to the gate of drive transistor 11b)). The Examiner reasons "[t]he motivation to modify Uchino with Seto arises from the stated desire to use a conventional drive circuit without increasing power consumption." *Id.* at 4 (citing Seto ¶ 36).

Appellant contends, for a variety of reasons, there is no motivation for adding Seto's storage capacitor 11d to Uchino's circuit. App. Br. 6–7. In

particular, Appellant argues Uchino's capacitor (C211) is described by Uchino as a "'pixel capacitor Cs,' where the 's' usually stands for 'storage.'" *Id.* at 7 (citation(s) omitted). Appellant argues capacitor C211 of Uchino is a "storage capacitor" rather than a feedback capacitor as the Examiner asserts and, thus, adding Seto's storage capacitor "would be counter-intuitive," "redundant," "and therefore not obvious." *Id.* at 6. Appellant further asserts Uchino's capacitor C211 is clearly a "storage capacitor" because it is referred to in Uchino, at times, as "Cs" where "s" stands for storage. *Id.* at 7.

We are unpersuaded by Appellant's arguments. First, we note Appellant's assertion that "Cs" means "storage capacitor" is an unsupported assertion by Appellant's attorneys. It is well settled that mere attorney arguments and conclusory statements, which are unsupported by factual evidence, are entitled to little probative value. *In re Geisler*, 116 F.3d 1465, 1470 (Fed. Cir. 1997); *In re De Blauwe*, 736 F.2d 699, 705 (Fed. Cir. 1984). Attorney argument is not evidence. *In re Pearson*, 494 F.2d 1399, 1405 (CCPA 1974). Nor can such argument take the place of evidence lacking in the record. *Meitzner v. Mindick*, 549 F.2d 775, 782 (CCPA 1977).

The Examiner finds, and we agree, Uchino's capacitor C211 in Figure 13 is connected exactly as is required of the feedback capacitor recited by claim 1, i.e., between a gate of the drive transistor 211 (at node ND212) and the light emitting element 214 (at node ND211). *See* Ans. 7–8. Thus, structurally, and functionally, Uchino's capacitor C211 is identical to the recited "feedback capacitor."

Appellant argues "Seto's capacitor 11d is connected to a negative voltage source VB, but there is no such source in the Uchino Fig. 13 circuit,

so it is not clear where the other side of Seto's capacitor 11d would be connected if it were to be added to the Uchino circuit." App. Br. 6. We remain unpersuaded of Examiner error. The Examiner finds, and we agree, the claims do not recite another specific connection of the recited "storage capacitor" but, instead, merely recite "*a storage capacitor connected to the gate terminal of the drive transistor*." Ans. 6. Furthermore, Seto discloses precisely the recited electrical connection of a storage capacitor 11d (coupled between a stable voltage and the gate of the drive transistor) and the function of a storage capacitor ("a voltage according to the amount of charges stored in second capacitor element 11d of the holding circuit and applies a drive current to organic EL element 11a according to the voltage applied to the gate terminal"). Seto ¶ 51, Fig. 2; *see also* Ans. at 5–6.

Appellant further argues, for the first time in the Reply Brief, it would not be obvious to add Seto's storage capacitor to Uchino:

> [T]his would be diametrically opposed to the express teachings of Uchino. Specifically, Uchino's basic objective is to maintain a **constant** gate-to-source voltage Vgs of the drive transistor Vin. Uchino emphasizes the importance of this objective over and over again in his specification, and that objective would be defeated by making the changes proposed by the Examiner's argument because the gate-to-source voltage of the drive transistor would no longer be constant. Thus, the Examiner's proposed modification of the Uchino circuit is not only counter-intuitive, but goes against Uchino's express teachings. Uchino's teachings are also diametrically opposed to the present Applicant's teachings.

Reply Br. 2. Appellant directs attention to paragraphs 49 and 50 of Appellant's Specification that allegedly teach an objective to change the gate-to-source voltage, and conclude the "only motivation for adding the

second capacitor can be found in the present Applicant's teachings." *Id.* at 2–3.

Appellant raises this argument, regarding conflicting/opposing objectives between Uchino and Seto, for the first time in the Reply Brief. Appellant could have presented this argument in the Appeal Brief, such that the Board would have had the benefit of the Examiner's evaluation of the arguments in the responsive Answer. Appellant does not explain what good cause there might be to consider the new argument. Appellant's new argument is thus untimely and has, accordingly, not been considered. 37 C.F.R. § 41.41(b)(2); *see also Ex parte Borden*, 93 USPQ2d 1473, 1474 (BPAI 2010) (informative).

For the reasons discussed *supra*, we are unpersuaded of Examiner error. Accordingly, we sustain the Examiner's rejection of independent claim 1 and, for similar reasons, the rejection of independent claim 20, which contains similar limitations and is argued together with claim 1. App. Br. 7. Additionally, we sustain the Examiner's rejections of dependent claims 2–13, 15–19, and 21, which are not argued separately with particularity. *Id.* at 7, 9–10.

*Claims 22–43*

Independent claim 22 recites, in pertinent part, "a reset capacitor connected between the node and a reset line such that the reset line is capacitively coupled to the gate terminal of the drive transistor while the first switch transistor is turned on." The Examiner finds in Shibusawa a "first switch transistor TCT connected from drive transistor DRT's gate to a node in pixel circuit 18" and further finds an "unenumerated reset capacitor

capacitively coupling control line RG to the drive transistor DRT's gate." Final Act. 13 (citing Shibusawa, Fig. 9, ¶¶ 108, 116, 117).

Appellant argues, for a variety of reasons, "Shibusawa's line RG is not a reset line, and his unenumerated capacitor is not a reset capacitor." App. Br. 8.

We are unpersuaded the Examiner erred. Shown below is a portion of Shibusawa Figure 9 as annotated by the Examiner (Ans. 9) identifying the elements as the Examiner reads claim 22:

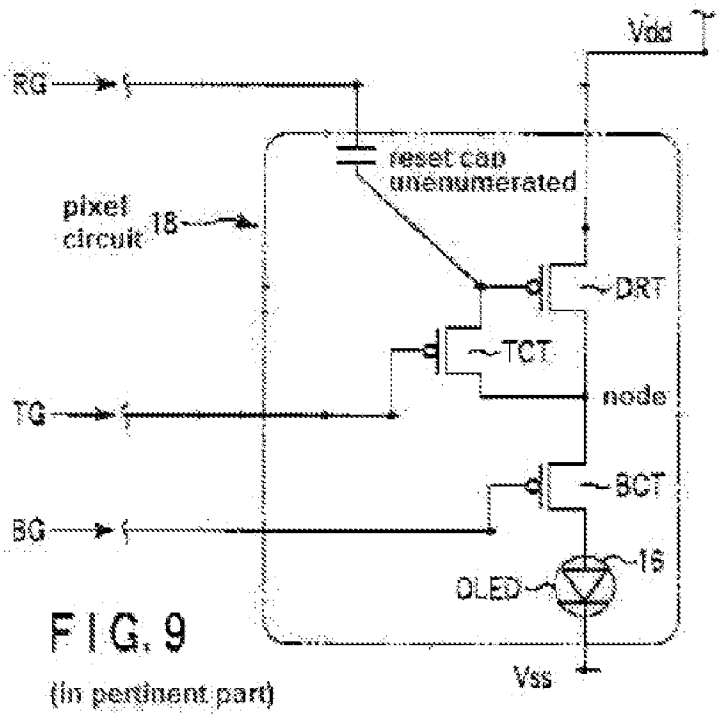


FIG. 9
(in pertinent part)

A portion of Shibusawa Figure 9 shown above, as annotated by the Examiner, illustrates drive transistor (DRT) having a gate terminal, first switch transistor (TCT) connected between the drive transistor's gate and a node of the pixel circuit, and reset capacitor ("reset cap unenumerated") connected between the node and reset line (RG) and also connecting reset line (RG) to the gate terminal of DRT.

Specifically, Appellant argues the "unenumerated capacitor" is permanently connected to the gate of DRT and, thus, "[t]here is no switching transistor in that part of the Shibusawa circuit." App. Br. 8. We are unpersuaded of Examiner error. Claim 22 does not preclude the recited reset capacitor from connecting the reset line (RG) to the drive transistor's gate permanently. So long as the recited reset capacitor at least couples the reset line to the drive transistor gate while the switching transistor (TCT) is on, the claim limitation is met regardless of what other conditions cause such a connection. *See* Ans. 11.

Appellant further argues the node identified by the Examiner "is not connected to either side of Shibusawa's 'unenumerated capacitor,' as required by Applicant's claim 22 for the reset capacitor." App. Br. 8. We remain unpersuaded of Examiner error. As seen in the annotated portion of Figure 9 *supra*, the reset capacitor of Shibusawa is coupled (through TCT) to the identified node when TCT is turned on. The claim does not specify or preclude particular conditions that cause the reset capacitor to be so connected or disconnected. *See* Ans. 10.

When construing claim terminology during prosecution before the Office, claims are to be given their broadest reasonable interpretation consistent with the Specification, reading claim language in light of the Specification as it would be interpreted by one of ordinary skill in the art. *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004). In this case, Appellant's Specification is devoid of any limiting definition of particular requirements of the recited connections. Given the lack of a relevant limiting definition in Appellant's Specification, the Examiner broadly but reasonably construes claim 22, consistent with the Specification,

to encompass Shibusawa's connection between the reset line RG and the drive transistor DRT's gate and between RG and the identified node of the pixel circuit.

For the reasons discussed *supra*, we are unpersuaded of Examiner error with respect to claim 22. Accordingly, we sustain the Examiner's rejection of independent claim 22. For similar reasons, we sustain the rejection of claims 23–39 argued together with claim 1. *See* App. Br. 9.

However, regarding independent claim 40, we are persuaded the Examiner erred. Independent claim 40 is a method claim whose preamble recites structure similar to that of claim 22. The method steps include "turning on the first switch transistor to capacitively couple the reset line to the gate terminal of the drive transistor *only* while the first switch transistor is turned on" (emphasis added). We are, therefore, persuaded of Examiner error by Appellant's argument that the reset capacitor of Shibusawa does not connect the reset line to the drive transistor's gate terminal *only* when TCT is switched on. Claim 40 includes the limiting recitation "*only*" not found in the related recitations of claim 22. Here, we find the Examiner has failed to adequately explain how, nor are we able to ascertain that, Shibusawa teaches capacitively coupling the reset line RG to the drive transistor's gate terminal "*only* while the first switch transistor is turned on," as recited in claim 40.

Thus, on the record before us, we are persuaded the Examiner erred in rejecting independent claims 40 and claims 41–43 dependent therefrom. Therefore, we do not sustain the rejection of claims 40–43.

## DECISION

We affirm the Examiner's decision to reject claims 1–13 and 15–39.

We reverse the Examiner's decision to reject claims 40–43.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART